Author: Theju Bernard

ISL75051SRH High Performance 3A LDO Evaluation Board User Guide

Description

The ISL75051SRH is a high-performance, adjustable, low-voltage, high-current, low-dropout linear regulator specified at 3A rated output current for input voltages from 2.2V to 6V. The LDO outputs can be adjusted from 0.8V to 5V by means of two preset resistors. Salient features of the part include:

- TID, ELDRS and SEE Rated
- Very Fast Load Transient Response
- ±2.0% Guaranteed VOUT Accuracy over Line, Load and Temperature
- Typical Dropout of 287mV at 3A
- EN Feature
- PG Feature
- OCP Feature
- Short-circuit and Over-temperature Protection

The ISL75051SRHEVAL1Z evaluation board provides a simple platform to evaluate performance of the ISL75051SRH. The device output voltage is adjustable, and jumpers are provided to easily set popular output voltages.

What's Inside

The evaluation kit contains the following:

- ISL75051SRHEVAL1Z evaluation board
- ISL75051SRH datasheet
- AN1667 application note

Test Steps

1. Select the desired output voltage by shorting one of the jumpers from J2 through J6. The option of JP7 provides for continuous adjustment of VOUT using potentiometer R13.
2. Set the OCP limit by using jumpers JP8 and JP9. JP9 = 0.8A min, and JP8 = 4A min.
3. Close JP10. Also closing jumper JP1 (2 and 3) selects R2 = 5.49k as pull-up for PGOOD.
4. Ensure that the output capacitor and C_P are set according to recommended values shown in Table 1.
5. Connect the input supply to VIN/GND and the load to VOUT/GND. Select the VIN to VOUT ratio to keep dissipation within the thermal limits of the device.
6. Use JP11 to enable/disable the IC; Open = Enable, and Close = Disable. (Note: For REVB boards, Close = Enable and Open = Disable.)

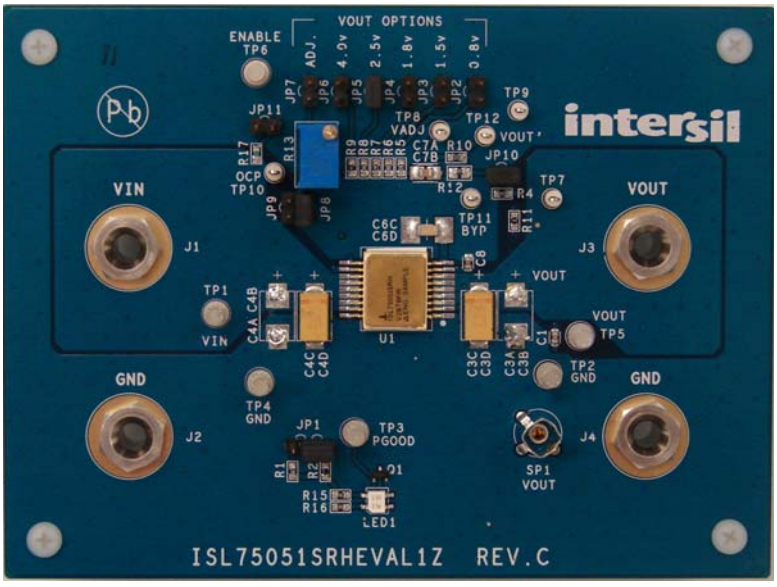


FIGURE 1. ISL75051SRHEVAL1Z EVALUATION BOARD

Optimizing LDO Performance

Performance of the ISL75051SRH can be optimized by following the guidelines provided in this application note.

Input and Output Capacitor Selection

RH operation requires the use of a combination of tantalum and ceramic capacitors to achieve a good volume-to-capacitance ratio. The recommended combination is a 220µF, 25mΩ, 10V DSSC 04051-032 rated tantalum capacitor in parallel with a 0.1µF MIL-PRF-49470 CDR04 ceramic capacitor. This is to be connected between VIN to GND pins and VOUT to GND pins of the LDO, with PCB traces no longer than 0.5cm. The stability of the device depends on the capacitance and ESR of the output capacitor. The usable ESR range for the device is 6mΩ to 100mΩ. At the lower limit of ESR = 6mΩ, the phase margin is about 51°C. On the high side, an ESR of 100mΩ is found to limit the gain margin at around 10dB. The typical GM/PM seen on the ISL75051SRHEVAL1Z evaluation board for VIN = 3.3V, VOUT = 1.8V, and IOUT = 3A, with a 220µF, 10V, 25mΩ capacitor, is GM = 16.3dB and PM = 69.16°C.

Pole Capacitor (C_P)

A small capacitor (C_P) can be placed on the ADJ pin of the ISL75051SRH, as shown in Figure 2, across the bottom resistor in the feedback resistor divider. This is effectively a pole. The value of the capacitor can be calculated using Equation 1:

$$F_P = 1/(2 \bullet pi \bullet R_{BOTTOM} \bullet C_P) \quad \text{(EQ. 1)}$$

The pole should be set to have the break frequency at 1MHz.

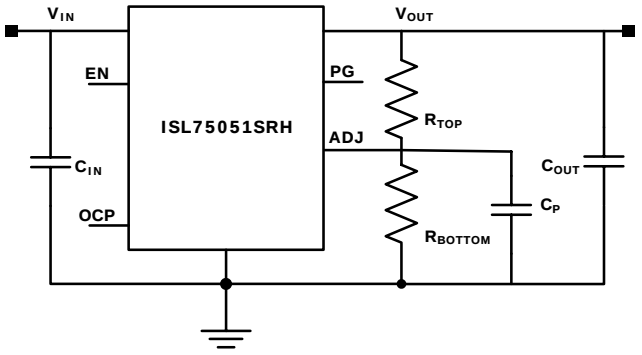


FIGURE 2. ISL75051SRH TYPICAL APPLICATION

Table 1 gives the recommended values for output capacitors (MLCC X5R/X7R) and C_P for different voltage rails. Correct selection of the output capacitor and C_P also helps increase PSRR at high frequencies. The board, however, uses a 100pF capacitor as a typical value most suited for the application range.

TABLE 1. RECOMMENDED OUTPUT CAPACITOR VALUES

V_{OUT} (V)	R_{TOP} (kΩ)	R_{BOTTOM} (Ω)	C_P (pF)	C_{OUT} (µF)
5.0	4.32	499	120	220
4.0	4.32	634	120	220
2.5	4.32	1.13k	120	220
1.8	4.32	1.74k	100	220
1.5 (Note 1)	4.32	2.26k	100	47
1.5	4.32	2.26k	100	220
0.8	4.32	7.87k	68	220

NOTE:

1. Either option could be used depending on cost/performance requirements.

Layout Guidelines

Good PCB layout is important to achieving expected performance. When placing components and routing traces, minimize ground impedance and keep parasitic inductance low. Give the input and output capacitors a good ground connection, and place them as close to the IC as possible. Route the traces connecting the ADJ pin away from noisy planes and traces, and keep the board capacitance of the ADJ net to GND as low as possible.

Thermal Guidelines

If the die temperature exceeds +175°C typical, then the LDO output shuts down to zero until the die temperature cools to +155°C typical. The level of power combined with the thermal impedance of the package (RTHjc of 4°C/W for the 18 Ld CDFP package) determines whether the junction temperature exceeds the thermal shutdown temperature specified in the “Electrical Specifications” table of the ISL75051SRH datasheet. Mount the device on a high effective thermal conductivity PCB with thermal vias, per JESD51-7 and JESD51-5. Place a silpad between package base and PCB copper plane. Select the VIN and VOUT ratios to ensure that dissipation for the selected VIN range keeps T_J within the recommended operating level of 150°C for normal operation.

Typical Performance Curves

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$.

FIGURE 3. START-UP WAVEFORMS: V_{IN} = 6.0V, V_{OUT} = 0.8V, EN LOW TO HIGH

FIGURE 4. START-UP WAVEFORMS: V_{IN} = 2.2V, V_{OUT} = 0.8V, EN LOW TO HIGH

FIGURE 5. SHUTDOWN WAVEFORM: V_{IN} = 6.0V, V_{OUT} = 0.8V, EN HIGH TO LOW

FIGURE 6. SHUTDOWN WAVEFORM: V_{IN} = 2.2V, V_{OUT} = 0.8V, EN HIGH TO LOW

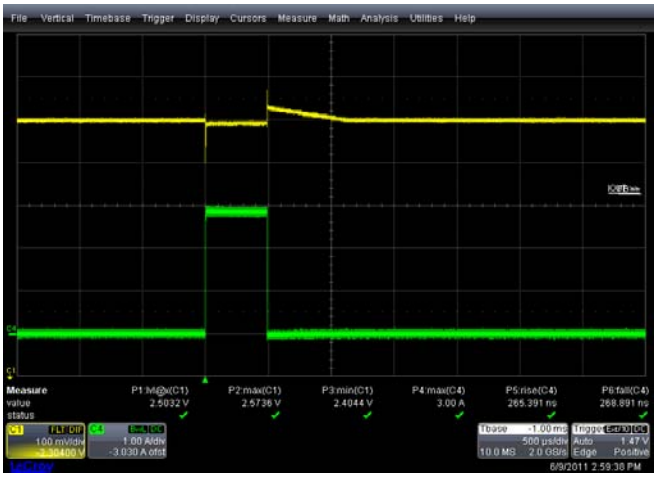


FIGURE 7. LOAD TRANSIENT, V_{IN} = 3.3V, V_{OUT} = 2.5V, C_{OUT} = 47µF 35mΩ

FIGURE 8. LOAD TRANSIENT, V_{IN} = 3.3V, V_{OUT} = 2.5V, C_{OUT} = 220µF 25mΩ

Typical Performance Curves

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$. **(Continued)**

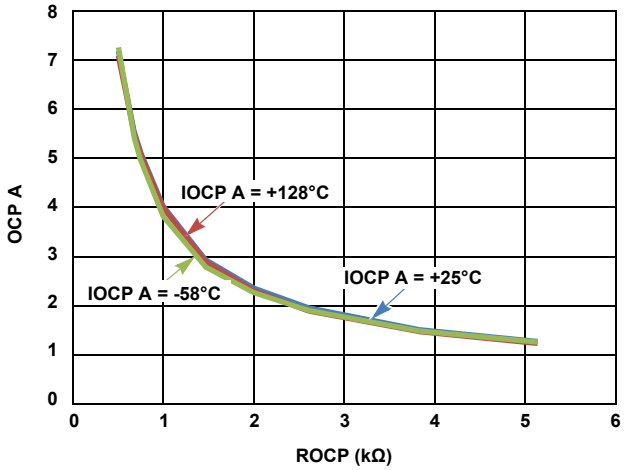


FIGURE 9. ROCP (kΩ) vs OCP A OVER TEMP

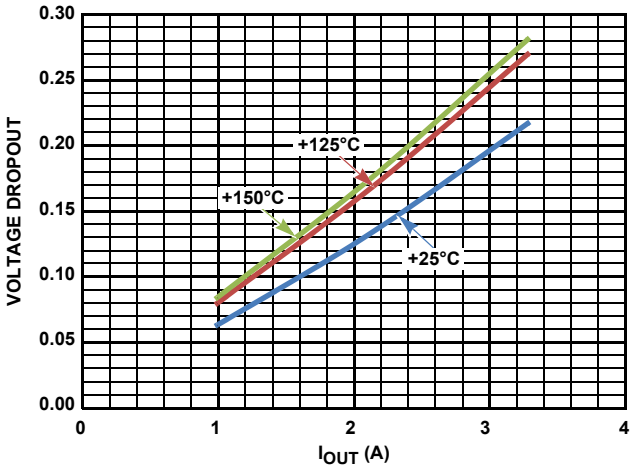


FIGURE 10. DROPOUT vs I_{OUT}

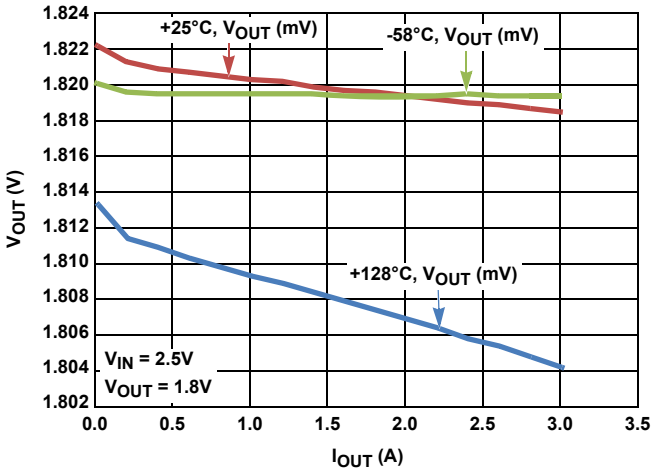


FIGURE 11. LOAD REGULATION V_{OUT} vs I_{OUT}

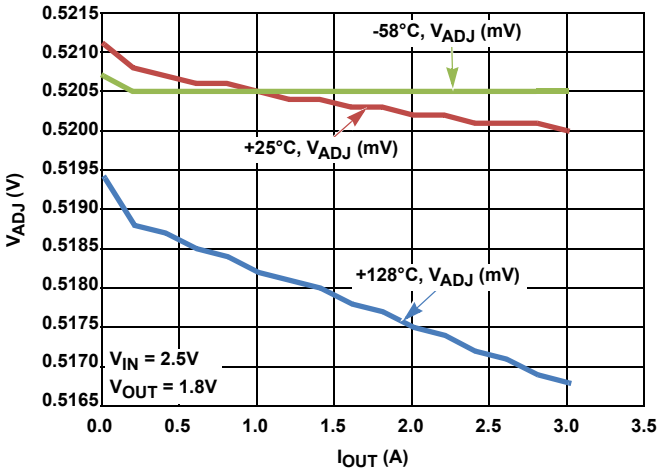


FIGURE 12. LOAD REGULATION V_{ADJ} vs I_{OUT}

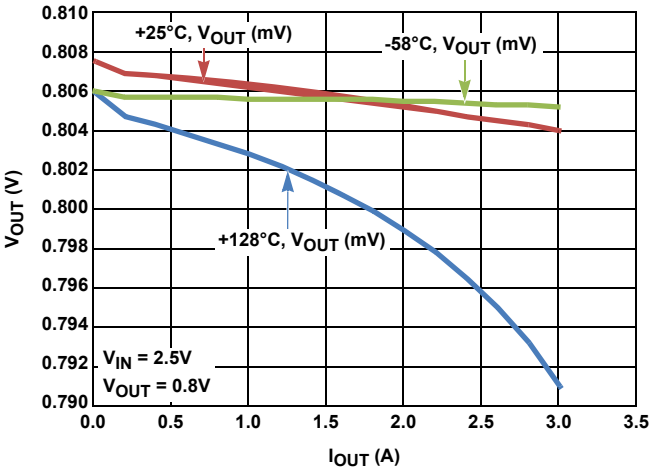


FIGURE 13. LOAD REGULATION V_{OUT} vs I_{OUT}

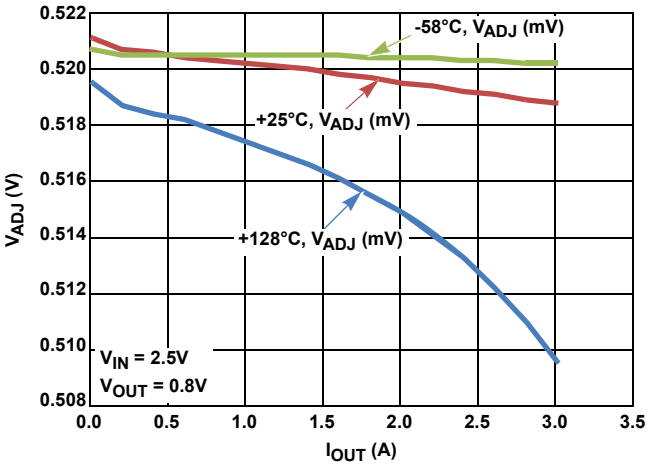


FIGURE 14. LOAD REGULATION V_{ADJ} vs I_{OUT}

Typical Performance Curves

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$. **(Continued)**

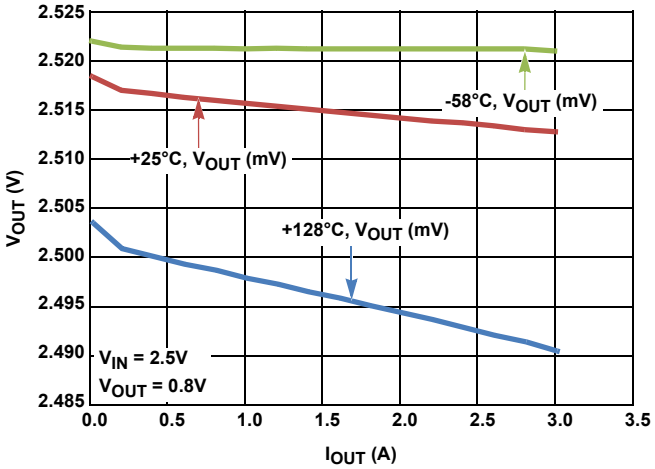


FIGURE 15. LOAD REGULATION V_{OUT} vs I_{OUT}

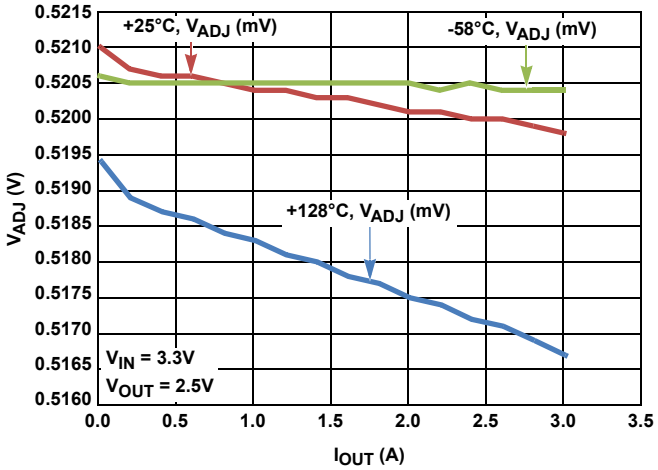
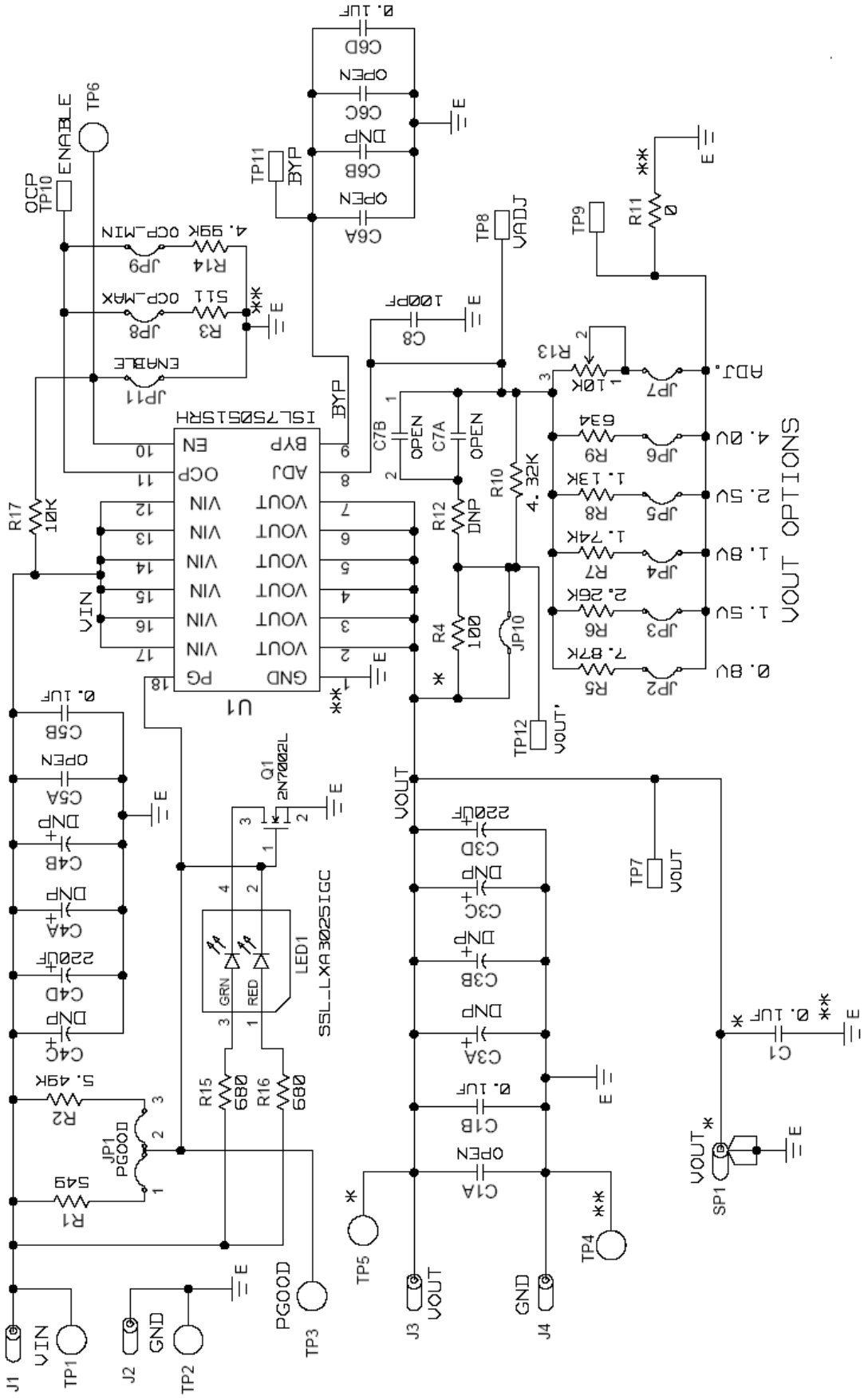


FIGURE 16. LOAD REGULATION V_{ADJ} vs I_{OUT}

Schematic


ISL75051SRH
U1
VIN
VOUT
GND
PGOOD
ENABLE
OCP
BYP
ADJ
VOUT OPTIONS
4.0V
2.5V
1.8V
1.5V
0.8V
ADJ.
LED1
SSL-LXA3025IGC
Q1
2N7002L
JP1
PGOOD
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
J1
J2
J3
J4
SP1
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
C1
C7A
C7B
C8
C1A
C1B
C3A
C3B
C3C
C3D
C4A
C4B
C4C
C4D
C5A
C5B
C6A
C6B
C6C
C6D
JP2
JP3
JP4
JP5
JP6
JP7
JP8
JP9
JP10
JP11
4.32K
DNP
OPEN
100
680
549
5.49K
4.99K
511
10K
634
1.74K
2.26K
7.87K
1.13K
0Ω
100PF
220UF
0.1UF

ISL75051SRHEVAL1Z Bill of Materials

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART
ISL75051SRHEVAL1ZREVCPCB	1	ea		PWB-PCB, ISL75051SRHEVAL1Z, REVC, ROHS	IMAGINEERING INC	ISL75051SRHEVAL1ZREV CPCB
C0805X472K5RACTU-T	1	ea	C7B	CAP, SMD, 0805, 4700pF, 50V, 10%, X7R, AEC-Q200, ROHS	KEMET	C0805X472K5RACTU
CDR04BX104AKWS	4	ea	C1B, C5B, C6B, C6D	CAP-MILQUAL, SMD, 1812, 0.1µF, 50V, 10%, X7R, ROHS	AVX	CDR04BX104AKWS
H1045-00101-50V5-T	1	ea	C8	CAP, SMD, 0603, 100pF, 50V, 5%, C0G, ROHS	PANASONIC	ECJ-1VC1H101J
H1045-00104-16V10-T	1	ea	C1	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS	MURATA	GRM39X7R104K016AD
H1045-DNP	0	ea	C1A, C5A, C6A, C6C	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
H1046-DNP	0	ea	C7A	CAP, SMD, 0805, DNP-PLACE HOLDER, ROHS		
T525D227M010ATE025	2	ea	C3D, C4D	CAP-TANT, SMD, 7.3x4.3, 220µF, 10V, 20%, 25mΩ, DF:10, ROHS	KEMET	T525D227M010ATE025
108-0740-001	4	ea	J1-J4	CONN-JACK, BANANA-SS-SDRLESS, VERTICAL, ROHS	JOHNSON COMPONENTS	108-0740-001
131-4353-00	1	ea	SP1	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS	TEKTRONIX	131-4353-00
1514-2	6	ea	TP1-TP6	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE	1514-2
5002	6	ea	TP7-TP12	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	5002
68000-236HLF-1X3	1	ea	JP1	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
69190-202HLF	10	ea	JP2-JP11	CONN-HEADER, 1x2, RETENTIVE, 2.54mm, 0.230 x 0.120, ROHS	BERG/FCI	69190-202HLF
SSL-LXA3025IGC-TR	1	ea	LED1	LED, SMD, 3x2.5mm, 4P, RED/GREEN, 12/20MCD, 2V	LUMEX	SSL-LXA3025IGC-TR
ISL75051SRH	1	ea	U1 (SEE ASSEMBLY INSTRUCTIONS)	IC-3A RAD HARD LDO REGULATOR, 18P, CDFP, ROHS	INTERSIL	ISL75051SRH
2N7002LT1G-T	1	ea	Q1	TRANSISTOR-MOS, N-CHANNEL, SMD, SOT23, 60V, 115mA, ROHS	ON SEMICONDUCTOR	2N7002LT1G

ISL75051SRHEVAL1Z Bill of Materials (Continued)

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART
3299W-1-103LF	1	ea	R13	POT-TRIM, TH, 3P, 10k, 1/2W, 10%, 3/8SQ, 25TURN, TOPADJ, ROHS	BOURNS	3299W-1-103LF
H2511-00R00-1/10W-T	1	ea	R11	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL	CR0603-10W-000T
H2511-01000-1/10W1-T	1	ea	R4	RES, SMD, 0603, 100Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1000FT
H2511-01002-1/10W1-T	1	ea	R17	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	KOA	RK73H1JT1002F
H2511-01131-1/10W1-T	1	ea	R8	RES, SMD, 0603, 1.13k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-071K13L
H2511-01741-1/10W1-T	1	ea	R7	RES, SMD, 0603, 1.74k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF1741V
H2511-02261-1/10W1-T	1	ea	R6	RES, SMD, 0603, 2.26k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-072K26L
H2511-02671-1/10W1-T	0	ea	R12	RES, SMD, 0603, 2.67k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-072K67L
H2511-04321-1/10W1-T	1	ea	R10	RES, SMD, 0603, 4.32k, 1/10W, 1%, TF, ROHS		
H2511-04991-1/10W1-T	1	ea	R14	RES, SMD, 0603, 4.99k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF4991V
H2511-05110-1/10W1-T	1	ea	R3	RES, SMD, 0603, 511Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5110FT
H2511-05490-1/10W1-T	1	ea	R1	RES, SMD, 0603, 549Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5490FT
H2511-05491-1/10W1-T	1	ea	R2	RES, SMD, 0603, 5.49k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5491FT
H2511-06340-1/10W1-T	1	ea	R9	RES, SMD, 0603, 634Ω, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-07634RL
H2511-06800-1/10W1-T	2	ea	R15, R16	RES, SMD, 0603, 680Ω, 1/10W, 1%, TF, ROHS	ROHM	MCR03EZPFX6800
H2511-07871-1/10W1-T	1	ea	R5	RES, SMD, 0603, 7.87k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-077K87L
4-40X1/2-SCREW	4	ea	Four corners	SCREW, 4-40x1/2in, PAN, NYLON, PHILLIPS, ROHS		
4-40X3/4-STANDOFF	4	ea	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX, NYLON, ROHS	KEYSTONE	1902D
5X8-STATIC-BAG	1	ea	Place assy in bag.	BAG, STATIC, 5x8, ZIPLOC, ROHS	INTERSIL	212403-013
ASSEMBLY INSTRUCTIONS	1	ea	a) U1 - Cut a 0.4 inch square of part # SP2000-0.020-AC-1212-NA	Instructions for assembly.	INTERSIL	ASSEMBLY INSTRUCTIONS
ASSEMBLY INSTRUCTIONS	1	ea	b) Affix to PCB where U1 will be installed.	Instructions for assembly.	INTERSIL	ASSEMBLY INSTRUCTIONS

ISL75051SRHEVAL1Z Bill of Materials (Continued)

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART
ASSEMBLY INSTRUCTIONS	1	ea	c) HAND SOLDER U1 on top of insulation	Instructions for assembly.	INTERSIL	ASSEMBLY INSTRUCTIONS
ASSEMBLY INSTRUCTIONS	1	ea	d) Wash after soldering	Instructions for assembly.	INTERSIL	ASSEMBLY INSTRUCTIONS
DNP	0	ea	C3A, C3C, C4A, C4C (6TPF220ML)	DO NOT POPULATE OR PURCHASE		
LABEL-DATE CODE	1	ea		LABEL-FOR DATE CODE AND BOM REV #	INTERSIL	LABEL-DATE CODE
SP2000-0.020-AC-1212-NA	0.3	ea	U1 (SEE ASSEMBLY INSTRUCTIONS)	INSULATION-SILICONE ELASTOMER, 12x12, 0.020in, W/ADHESIVE, ROHS	BERGQUIST	SP2000-0.020-AC-1212-NA

Layout

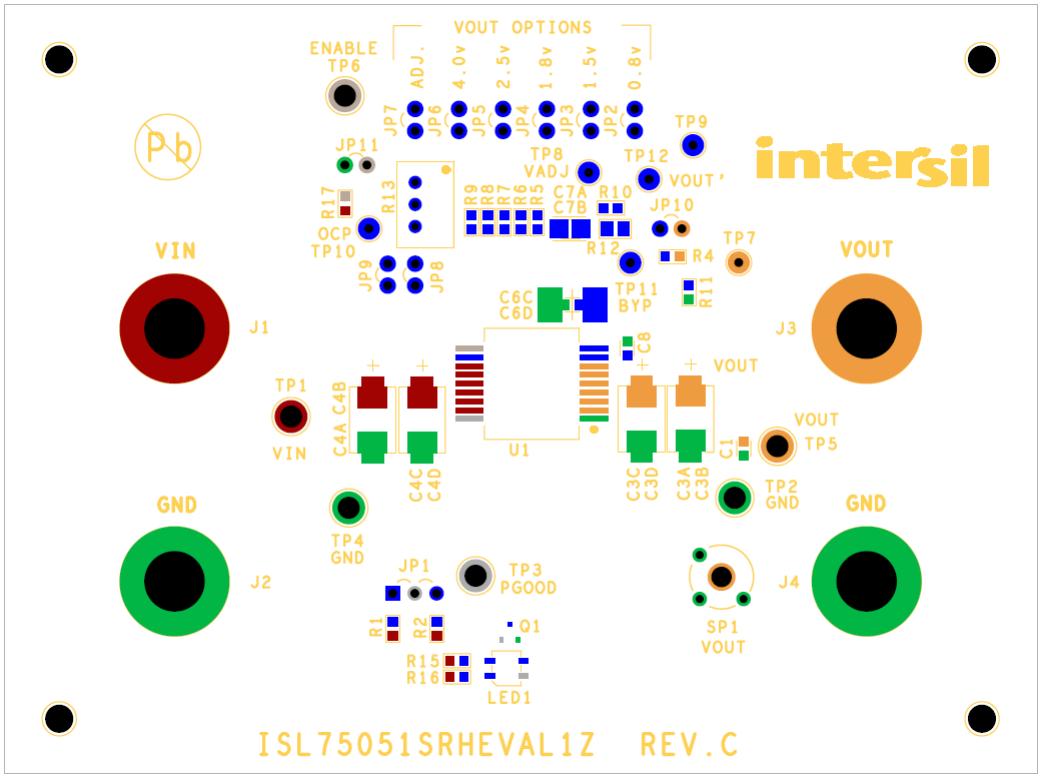


FIGURE 17. SILK SCREEN TOP

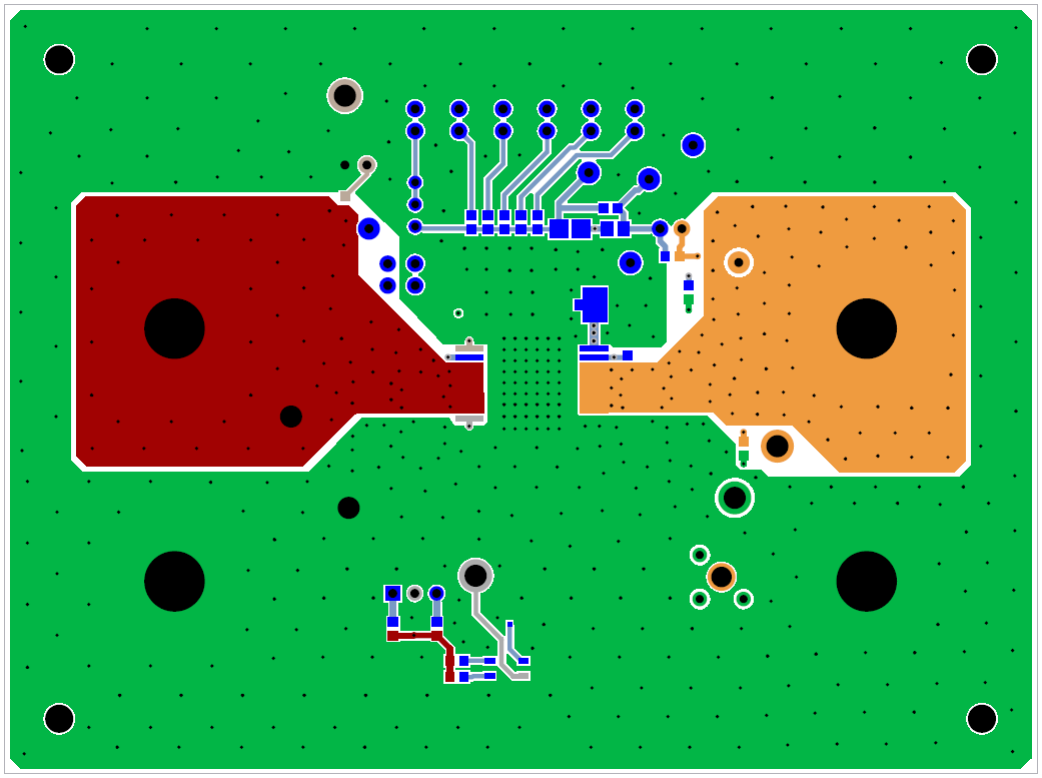


FIGURE 18. TOP LAYER COMPONENT SIDE

Layout (Continued)

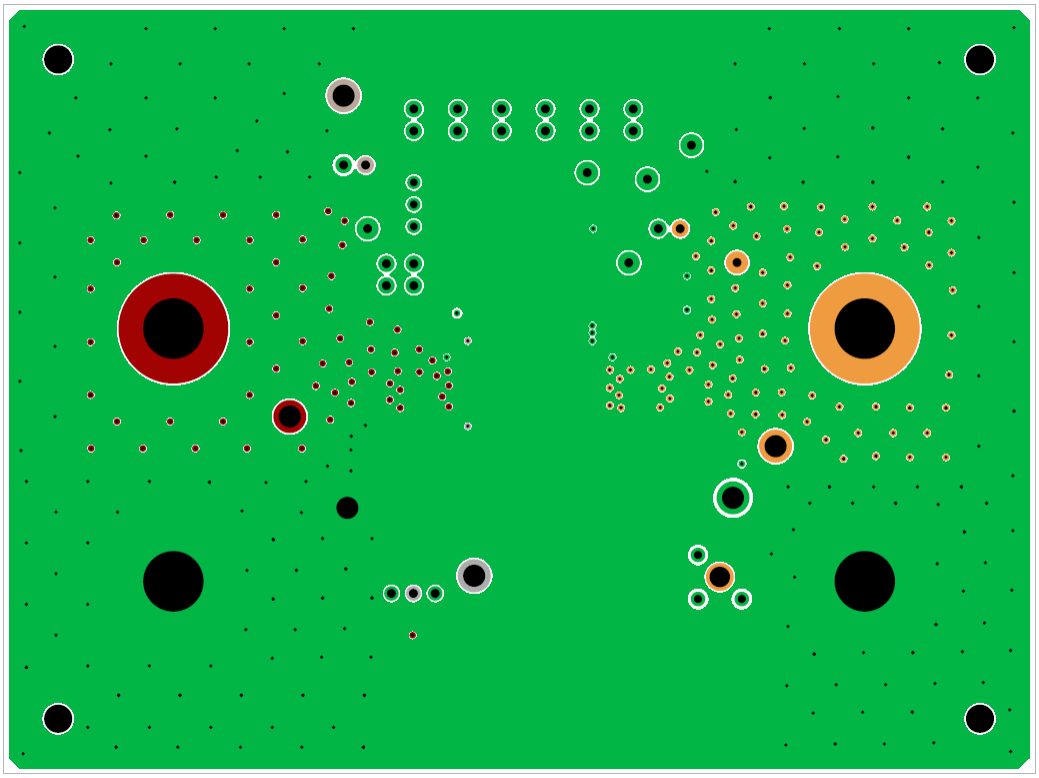


FIGURE 19. LAYER 2

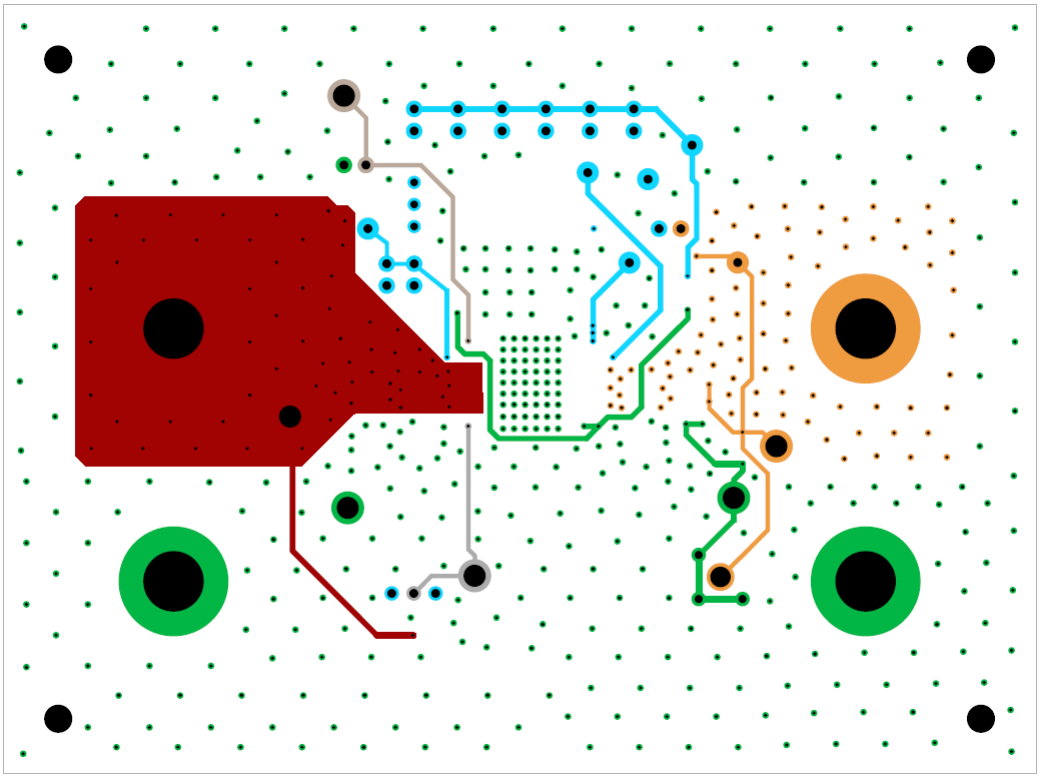


FIGURE 20. LAYER 3

Layout (Continued)

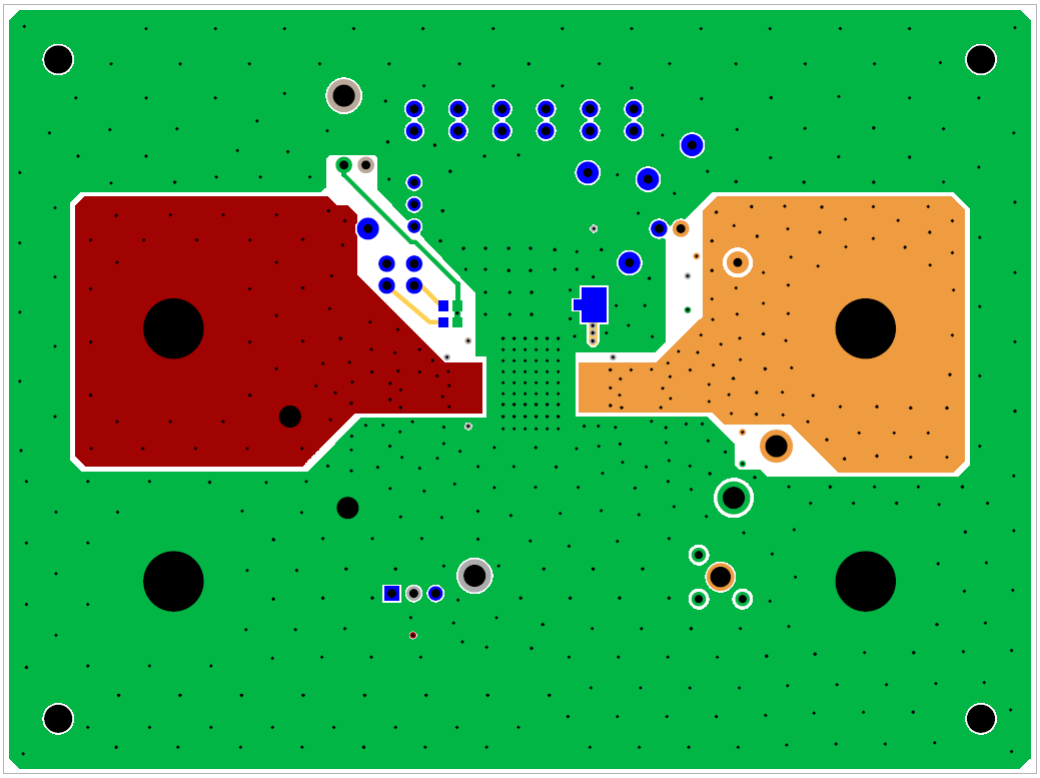


FIGURE 21. BOTTOM LAYER SOLDER SIDE

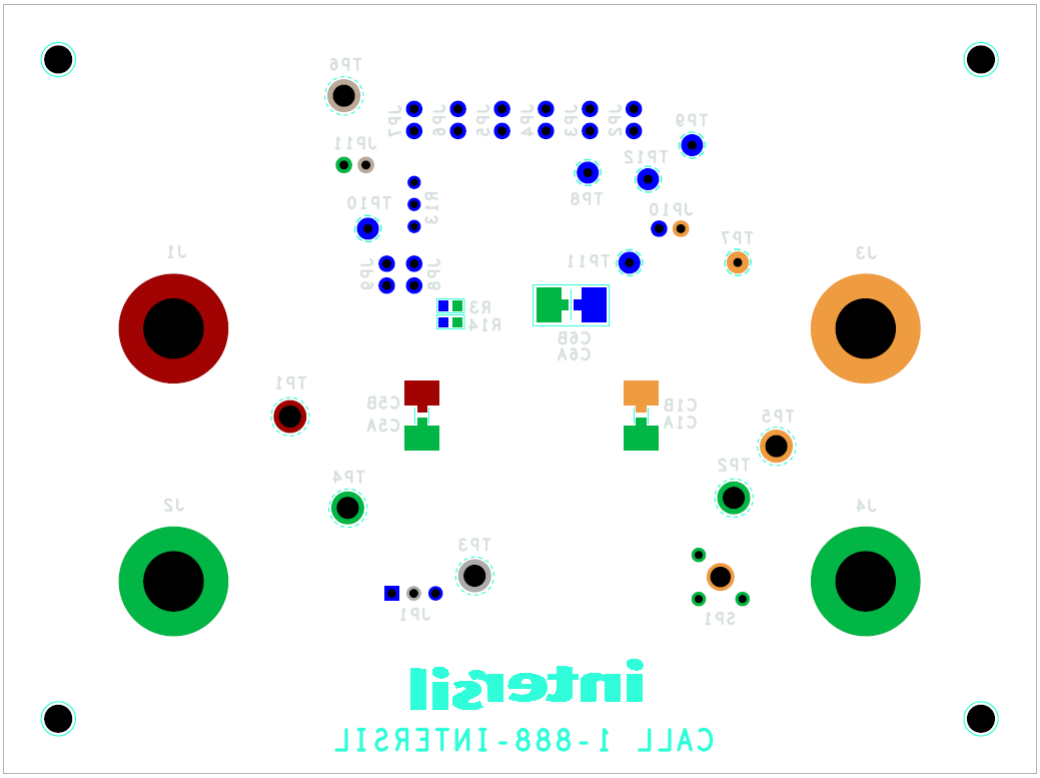


FIGURE 22. SILK SCREEN BOTTOM

Layout (Continued)

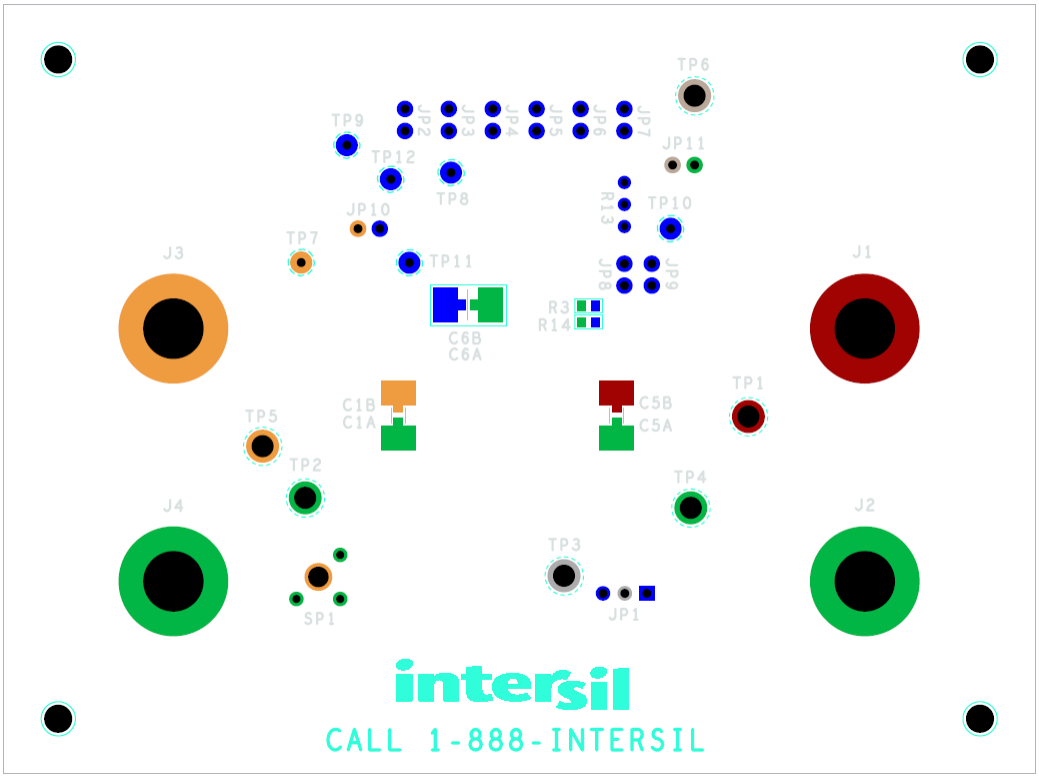
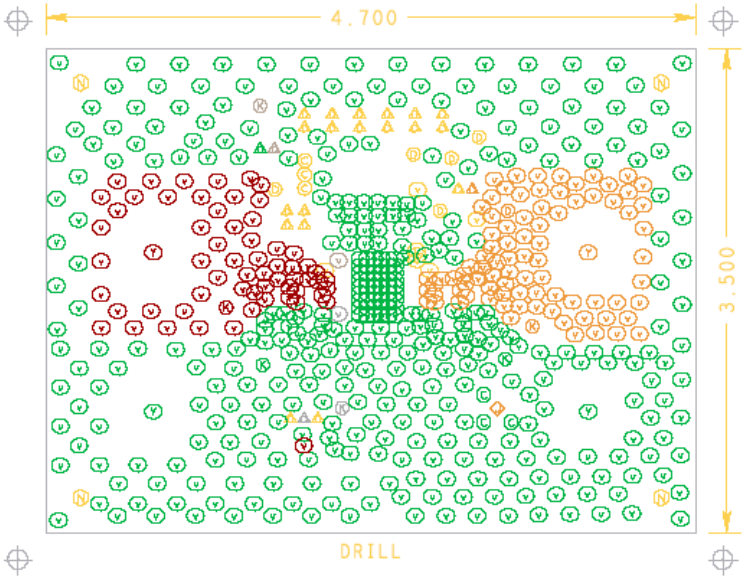


FIGURE 23. SILK SCREEN BOTTOM MIRROR

Drill Drawings



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
V	16.0	PLATED	547
C	35.0	PLATED	3
C	37.0	PLATED	3
D	40.0	PLATED	6
A	41.0	PLATED	23
B	93.0	PLATED	1
K	100.0	PLATED	6
Y	275.0	PLATED	4
N	128.0	NON-PLATED	4

NOTES:
1. THIS BOARD IS RoHS COMPLIANT.
2. PRINTED WIRING BOARD DESIGN AND ACCEPTANCE CRITERIA SHALL BE IAW WITH THE REQUIREMENTS OF IPC-D-275 AND IPC-A-600.
3. MATERIAL: FR4 (RoHS COMPLIANT), 1 OZ COPPER.
4. APPLY SOLDER MASK, BOTH SIDES OVER BARE COPPER IAW IPC-SM-840. CLASS 2 (LPI) (BLUE MASK).
5. ALL PATTERNS ARE VIEWED FROM THE PRIMARY SIDE LOOKING THROUGH THE BOARD.
6. UNLESS OTHERWISE SPECIFIED ALL HOLE DIAMETERS ARE AFTER PLATING.
7. APPLY SILKSCREEN USING WHITE NON-CONDUCTIVE EPOXY BASED INK.
8. PWB MUST BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY. USE NETLIST PROVIDED ISL75051SRHEVAL1ZC_IPC356.IPC IAW IPC-D-356.
9. MARK DATE CODE AND MANUFACTURES IDENIFICATION ON SOLDER SIDE PER IPC-6011 AND IPC-6012.
10 TOLERANCE ON ALL DRILL HOLES SHALL BE IAW IPC-D-2221 & 2222 UNLESS OTHERWISE SPECIFIED.

PHYSICAL BOARD DIMENSIONS
& LAYER STRUCTURE